22.6 A One-Cycle Lock Time Slew-Rate-Controlled Output Driver

Young-Ho Kwak[1], Inhwa Jung[1], Hyung-Dong Lee[2], Young-Jung Choi[2], Yogendera Kumar[1], Chulwoo Kim[1]

[1]Korea University, Seoul, Korea, [2]Hynix Semiconductor, Icheon, Korea

Increased data rates and signal frequencies have given rise to several effects, specifically, the large current produced by CMOS output drivers generate noise on the inductive bond wire and package and board traces. Moreover, inadequate termination and crosstalk are other serious noise sources. Shin et al. [1] propose a slew-rate controlled output driver using a PLL. After the PLL locks, the VCO bias voltage feeds the slew-rate control block to produce appropriate control signals, which are used to control the slew-rate. However, a PLL is a high-order system that may suffer from stability. Furthermore, a PLL consumes large area and high power, and it takes a long time to lock the system. For use in 1Gb/s DDR2 SDRAM, Matano et al. [2] propose a slew-rate controlled output driver. In that method, it takes tens of cycles to generate the slew-rate control signals. Recently an output driver using a speed-locked-loop (SLL) was proposed [3]. However, it still takes eight cycles for correct locking due to the feedback part of SLL.

In this work, an open-loop slew-rate controlled output driver with one-cycle lock time is proposed. By using an all-digital open-loop architecture, this output driver occupies low area and keeps the slew-rate constant, even with various PVT changes, with one-cycle lock time, which enables output-on-demand and reduces standby current while updating the control signal promptly.

A block diagram of the proposed slew-rate controlled output driver is shown in Fig. 22.6.1. The circuit is composed of three units: a PVT variation detector, a select signal generator, and a segmented output driver. The PVT variation detector detects process, voltage, and temperature variations. The select signal generator generates control signals using input from the PVT variation detector to decide the drive strength of the output driver. The last block is a segmented output driver that sends the input data signal to the output with a constant slew-rate.

Figure 22.6.2 shows the schematic and fundamental operation of the PVT variation detector. It consists of three blocks: a delay line, a digitizer, and a switching detector. An open loop circuit of delay cells forms the delay line and the digitizer quantizes the outputs of the delay cells. When the reference clock is fed to the circuit, a multi-phase clock is generated with a constant phase difference between delay cells. The delay resolution, τ, and the number of delay cells are dependent on the slew-rate and the process technology. The number of high state outputs of the delay line varies according to PVT variations. The digitizer using these multi-phase clock signals counts the number of high delay cell outputs, and the switching detector locates the place where input signal changes from low to high. Specifically, the switching detector identifies the last high delay cell. The output signal from the PVT variation detector feeds the select signal generator to produce the appropriate control signals. These control signals are then used to control the slew-rate of the output driver.

The β ratio (W_p/W_n) of the delay cell is kept the same as that of the segmented output driver, shown in Fig. 22.6.3, to match the PVT variations between the control block and the output driver. Since the delay cells are constructed with static inverters, they consume little power. The number of delay cells is set to 20 to satisfy and locate all PVT variation ranges in a given design specification.

The operation of the digitizer is shown in Fig. 22.6.2. The capturing the output of the delay cell at phase π indicates that the output signal is holding an arbitrary voltage between V_{DD} and ground. The digitizer quantizes this analog output from the delay cell into the digital value of '1' or '0' at the falling edge of the clock signal. Moreover, inverters are used at the output of each delay cell to prevent the load capacitance from changing when the D flip-flops of the *n*-bit registers switch. As a result, the delay time of each delay cell keeps the constant value τ. The outputs of the digitizer are fed to the switching detector. The primary role of the switching detector is to seek the switching location of the reference clock using NOR logic on inverted signals from the digitizer.

The select signal generator depicted in Fig. 22.6.3 illustrates that it uses output signals from the PVT variation detector to create on and off signals to control the segmented output driver. Figure 22.6.3 also shows the structure of the distributed and weighted output drivers. To keep the output impedance constant, three inverters (inv1, inv2, inv3) are selectively turned on according to the PVT variations. Moreover, six delay blocks are inserted in front of the inverters to prevent inverters from being turned on simultaneously, minimizing switching power noise. Inv1, inv2, and inv3 are turned on selectively by the select signal generator.

Simulation waveforms are shown at the top of Fig. 22.6.4 where the slew-rate of the output driver changes from 1.2V/ns to 2.4V/ns one cycle after the clock signal is fed to the PVT variation detector. Also, the simulated slew-rate of the output signals in response to the PVT variations (NN, FF, SS, SF, FS, 25˚C to 95˚C, 1.44V, 1.8V) is shown. In the output driver, the PMOS and NMOS transistors are controlled together to match the PVT variations of delay element and output driver. The waveforms show that output slew-rate for input data signal ranges from 2.1V/ns to 3.6V/ns. The measured slew-rate of 2.86V/ns with four different supply voltages is also shown at the bottom of Fig. 22.6.4.

Figure 22.6.5 shows the shmoo plot of the output driver, illustrating that the correct inverters among segmented inverters are selected to turn on for various PVT ranges. The voltage is subdivided into 17 values by varying ±2% of the nominal voltage. The temperature range was also divided by varying the temperature in 10˚C increments at a time, from 25˚C to 95˚C. For example, the symbol d, 2 shown in Fig. 22.6.5 indicates that the default inverter and inv2 turn on to attain desirable slew-rate in between 2.1 and 3.6V/ns. If the number of control signals increases from 3 bits to 4 or 5 bits, fine control is possible and then the range of slew-rate is narrowed.

A die micrograph of the proposed output driver fabricated in a 1P4M 0.18μm CMOS process is shown in Fig. 22.6.6. The die area of the slew-rate control block is 0.009mm^2. Figure 22.6.7 shows the comparison results of the proposed output driver with the conventional drivers. The proposed output driver control block consumes 0.013mW/Mb/s and occupies the least area. Also, it overcomes the shortcomings of previous output drivers. First, it is implemented with digital circuits only. This not only enables low power consumption but also reduces the chip area. The second advantage is that due to the open-loop and optimal architecture, only one cycle is needed for locking. Hence, output-on-demand is feasible and the slew-rate control block can be shut-down whenever necessary. The advantages mentioned above thus make proposed output driver widely applicable to applications such as PCI bus, DDR2, GDDR3, and UDMA100.

Acknowledgements:
This work was supported by the Hynix Semiconductor Inc.

References:
[1]S.-K. Shin, S.-M. Jung, J.-H. Seo, et al., "A Slew-Rate Controlled Output Driver Using PLL as Compensation Circuit," *IEEE J. Solid-State Circuits,* vol. 38, no. 7, pp. 1227-1233, Jul., 2003.
[2] T. Matano, Y. Takai, T. Takahashi, et al., "A 1-Gb/s/pin 512-Mb DDRII SDRAM Using a Digital DLL and a Slew-Rate-Controlled Output Buffer," *IEEE J. Solid-State Circuits,* vol. 38, no. 5, pp. 762-768, May, 2003.
[3] M. Bazes, "Output Buffer Impedance Control and Noise Reduction Using a Speed-Locked Loop," *ISSCC. Dig. Tech. Papers,* pp. 486-487, Feb., 2004.

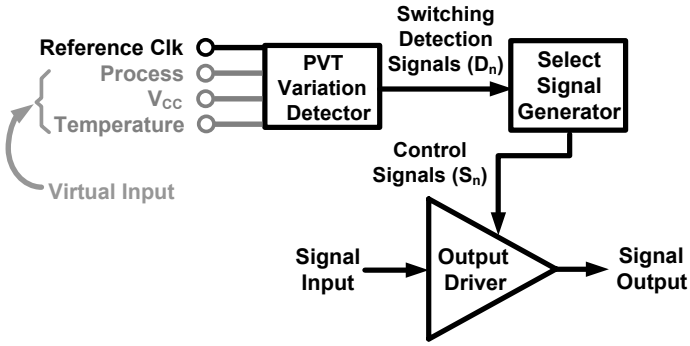

Figure 22.6.1: Proposed slew-rate controlled output driver's block diagram.

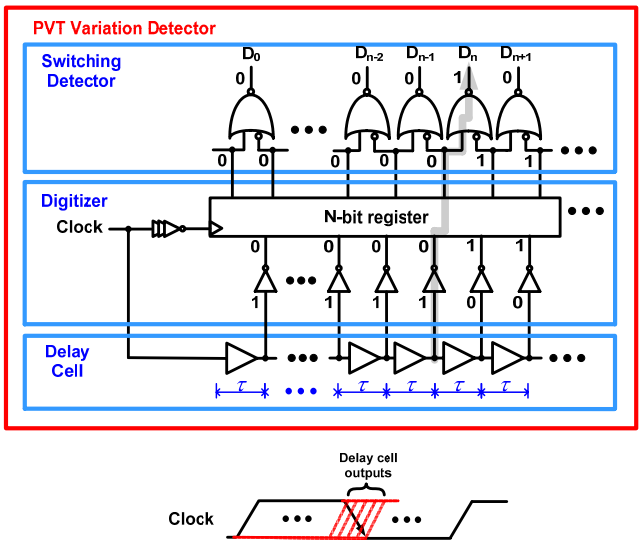

Figure 22.6.2: The schematic of PVT variation detector and the operation of digitizer.

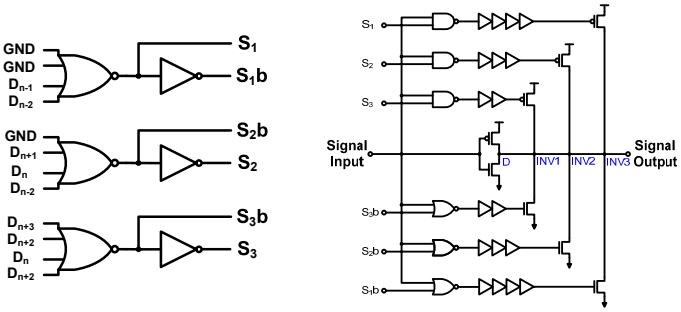

Figure 22.6.3: Schematics of select signal generator and weighted output driver.

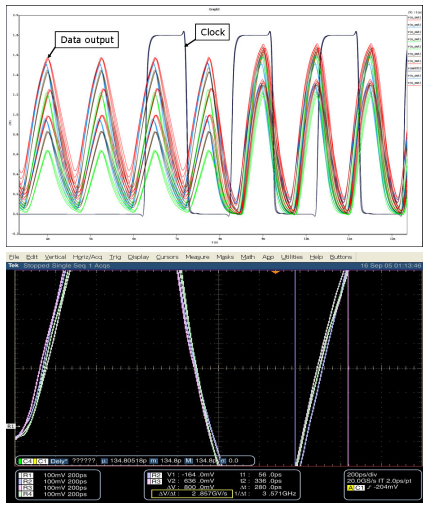

Figure 22.6.4: Simulation results of output-on-demand and constant slew rate with various PVT ranges (top) and the measured slew-rate with four different supply voltages (bottom).

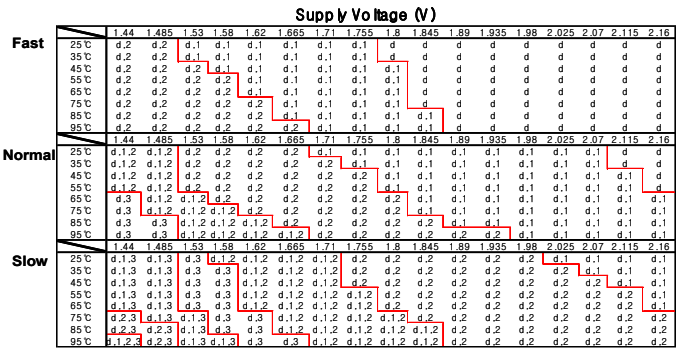

Figure 22.6.5: The Shmoo plot of proposed output driver.

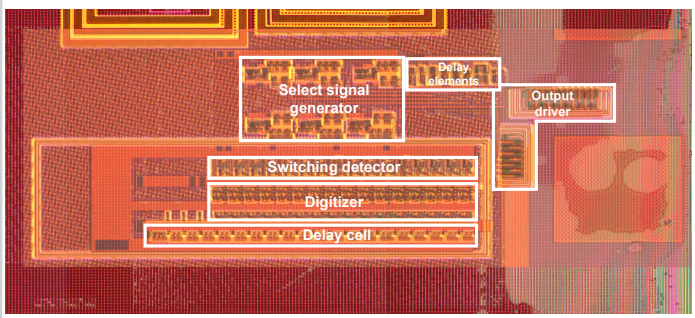

Figure 22.6.6: Die photo of the proposed output driver.

Continued on Page 611

	[1]	[2]	[3]	This work
Controller Type	Analog PLL	Mode/Digital Code	Digital SLL	Digital
Process	0.18um CMOS	0.13um CMOS	0.35um CMOS	0.18um CMOS
Operating Freq.	50Mbps	1Gbps	100Mbps	1Gbps
Power-down Mode	Difficult	Easy	Easy	Easiest
Lock Time	Hundreds of cycles	Tens of cycles	Several cycles	One cycle
Architecture	Closed loop	Closed loop	Closed loop	Open loop
Slew Spec.	0.4 -1 V/ns	2.0 – 4.0 V/ns	1.0 – 4.0 V/ns	2.0 – 4.0 V/ns
Slew Rate	0.403 – 0.99 V/ns	1.6 – 2.2 V/ns	-	2.1 – 3.58 V/ns
Supply	3.3 V	1.8 V	3.3 V	1.8 V
External Resistance	-	Yes	No	No
Power Consumption	-	-	Medium (2.2mW, 0.22mW/Mbps)	Low (13.7mW, 0.013mW/Mbps)
Controller Area	Large (0.16mm^2)	-	Medium (0.045mm^2)	Small (0.009mm^2)

Figure 22.6.7: The comparisons of conventional and proposed one.

